Name: Ningyuan Zhang

Section: A

Date: 2/21/2017

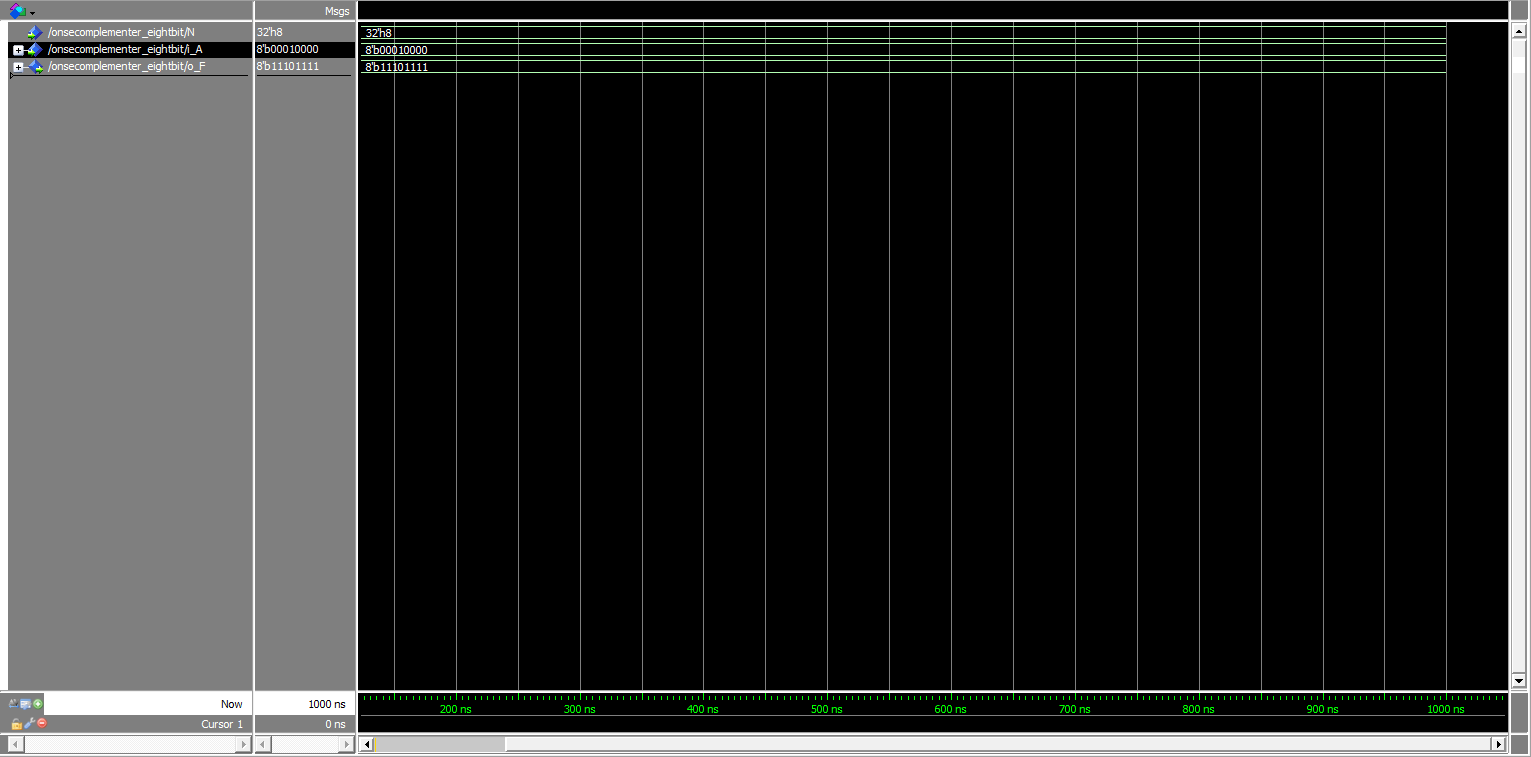
Instructor: Akhilesh Tyagi

Lab-5

1). One’s Complimenter

The code was included in file onescomplimenter\_eightbit.vhd

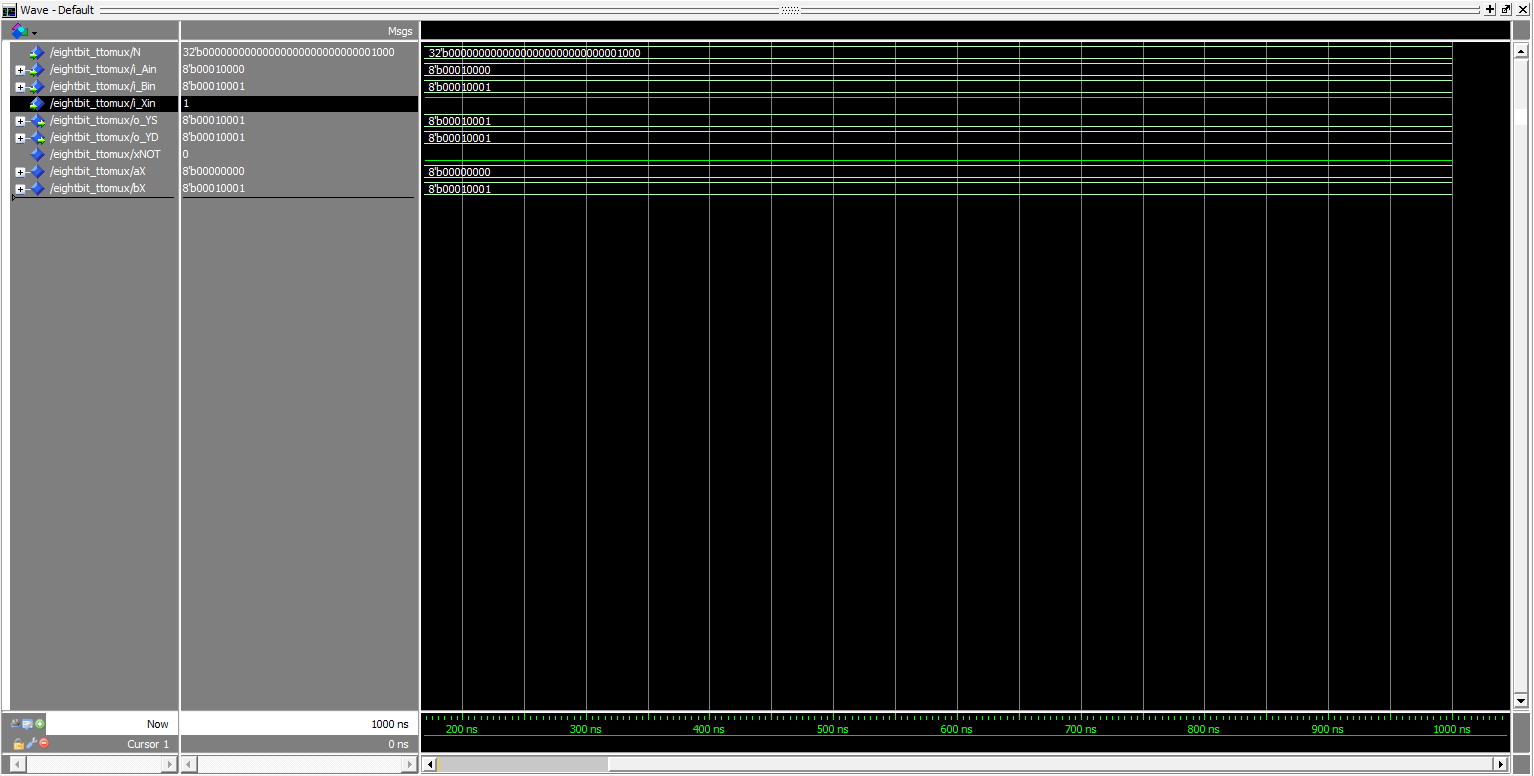
The wave form for the one’s complimenter:



2). Two-Input Multiplexer

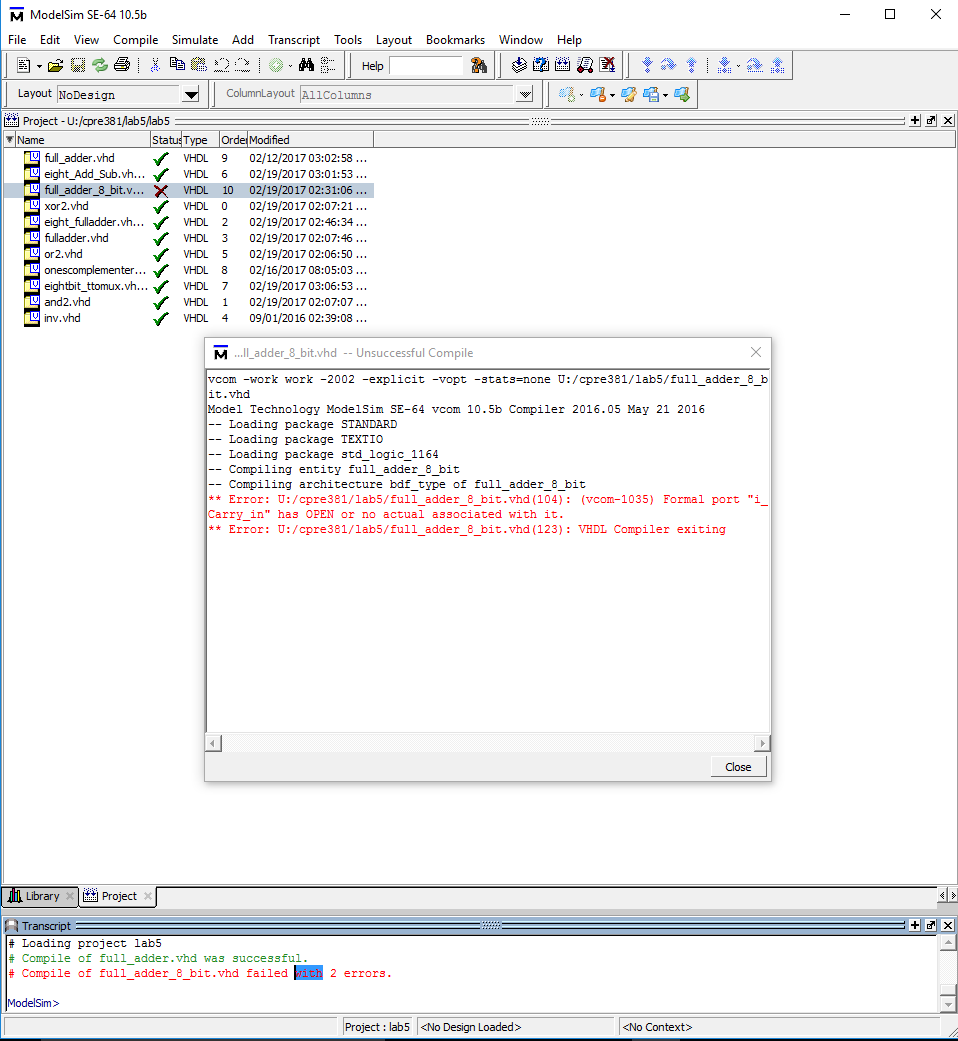
The code was included in file eightbit\_ttomux.vhd

The wave form of the ttomux is:



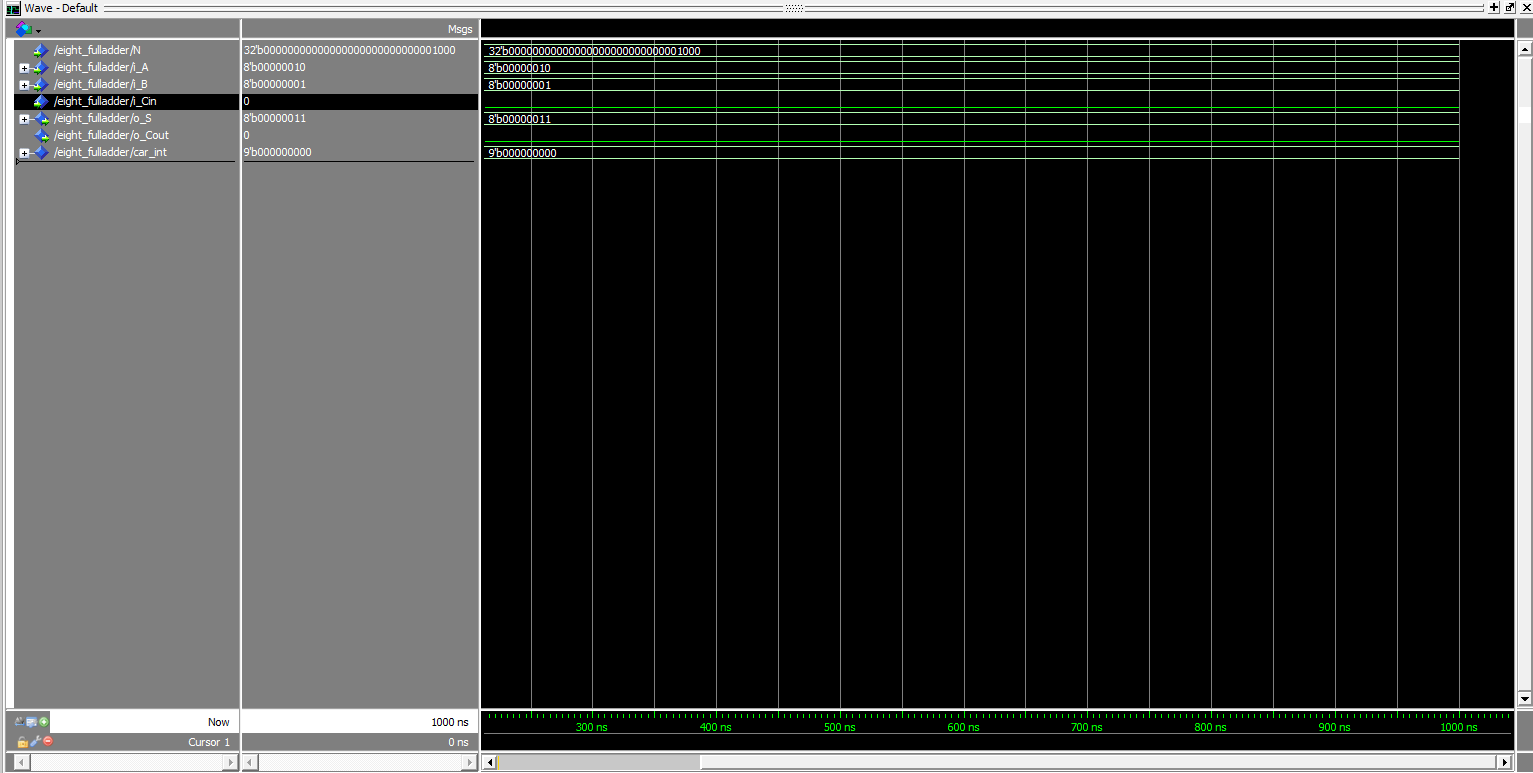
3) Full Adder

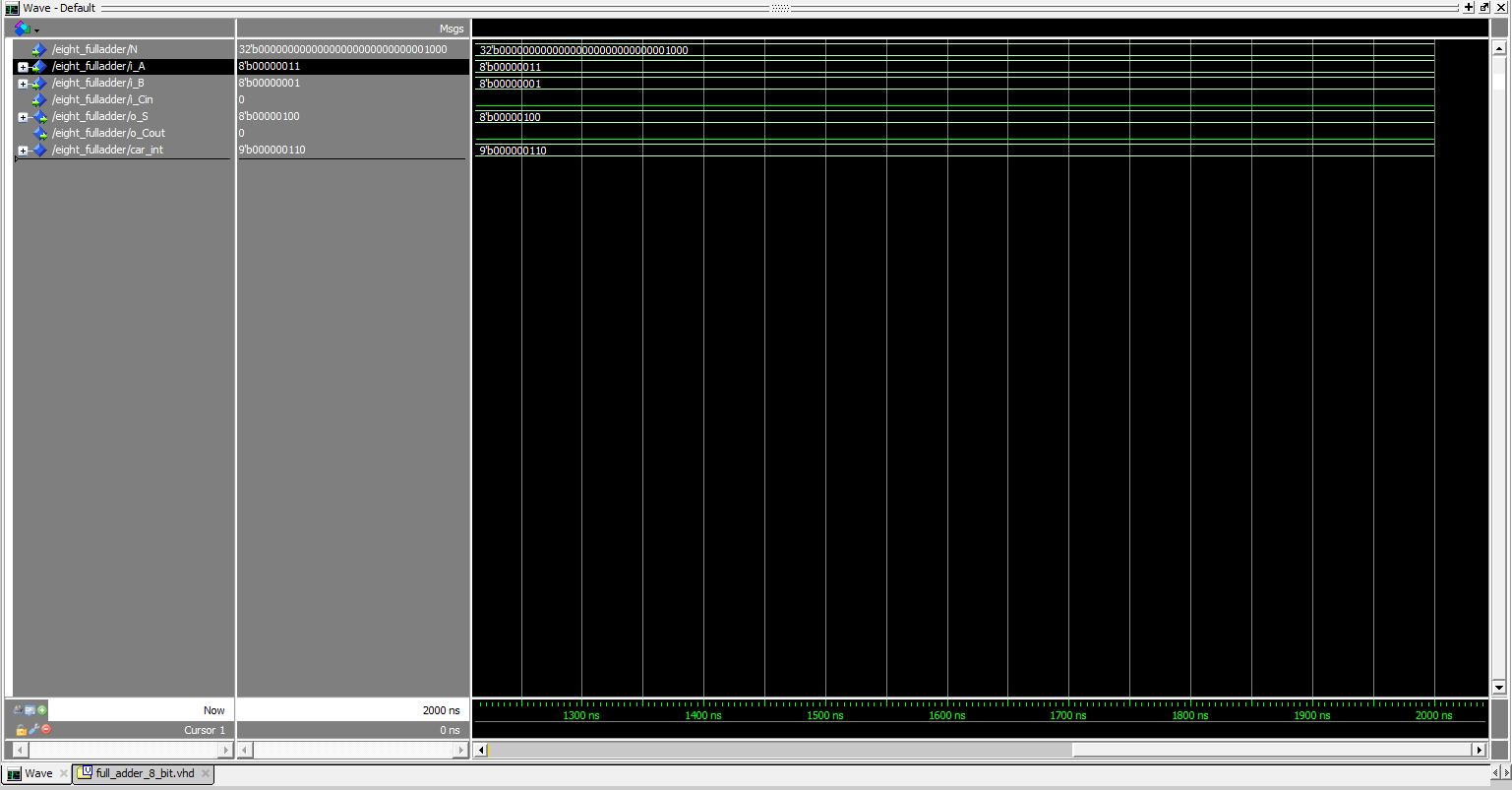
In this part, I failed to create VHDL file by my block diagram. I finished my Diagram and compiled it successfully, and did created the VHDL. the block diagram was named full\_adder\_8\_bit.bdf, and the vhdl file was named full\_adder\_8\_bit.vhd. but when I tried to simulate with modelsim, the vhdl file got error when compiling the file:

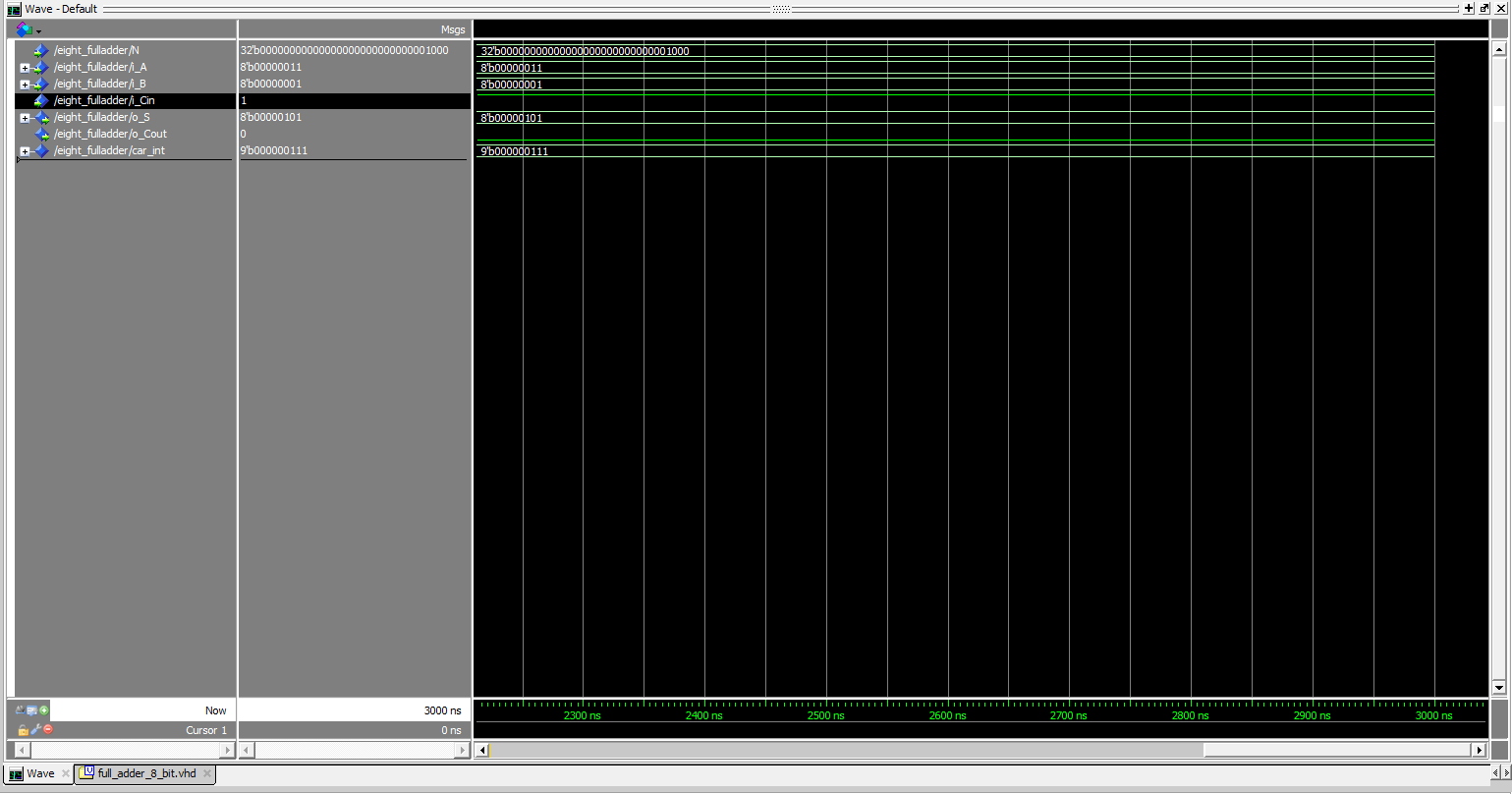


due to this problem, I used my own vhdl-only based file that I created which was named eight\_fulladder.vhd and generated a block named eight\_fulladder.bsf.

the tests of the program with waveforms:

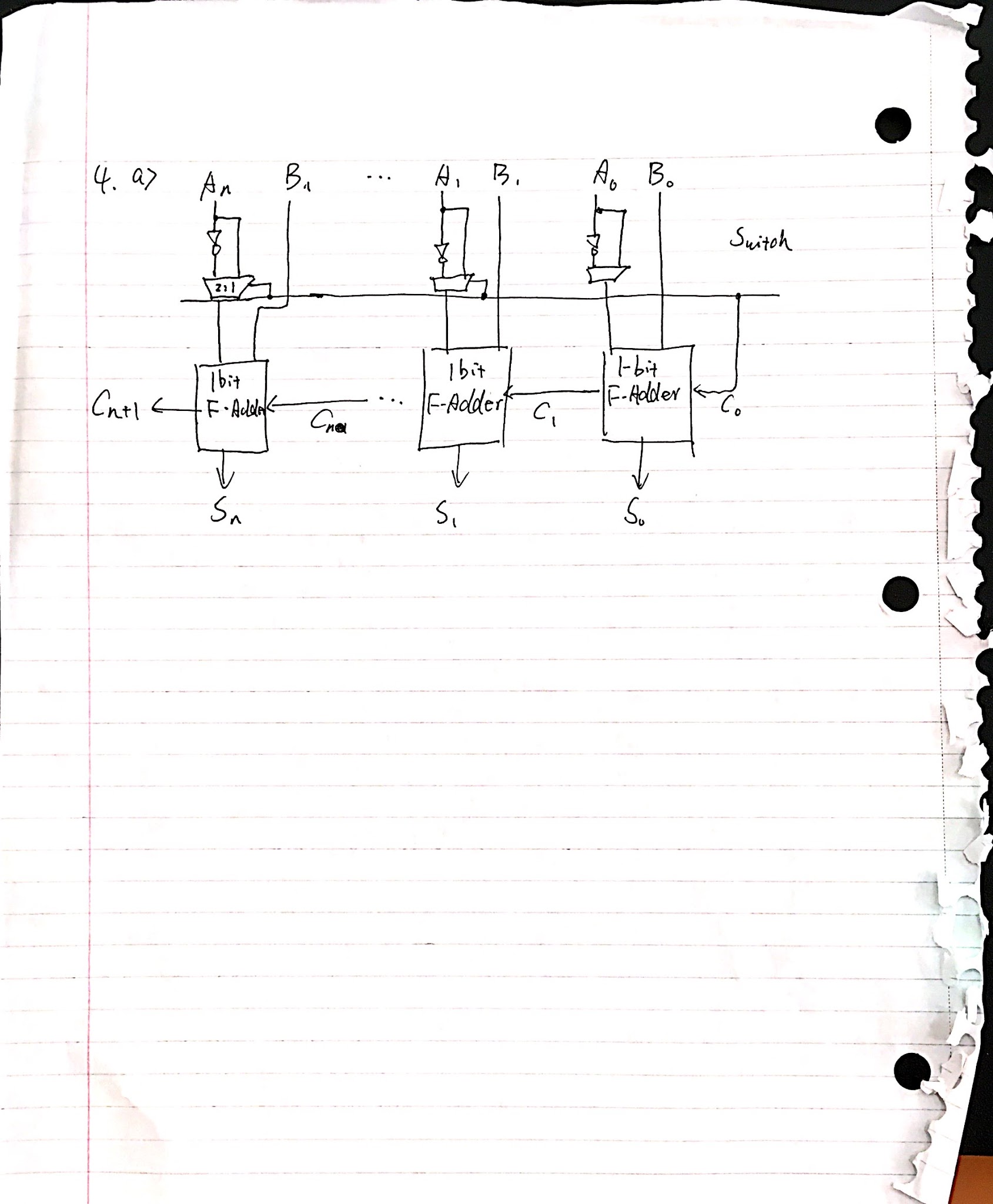






4). Adder/Subtractor with Control

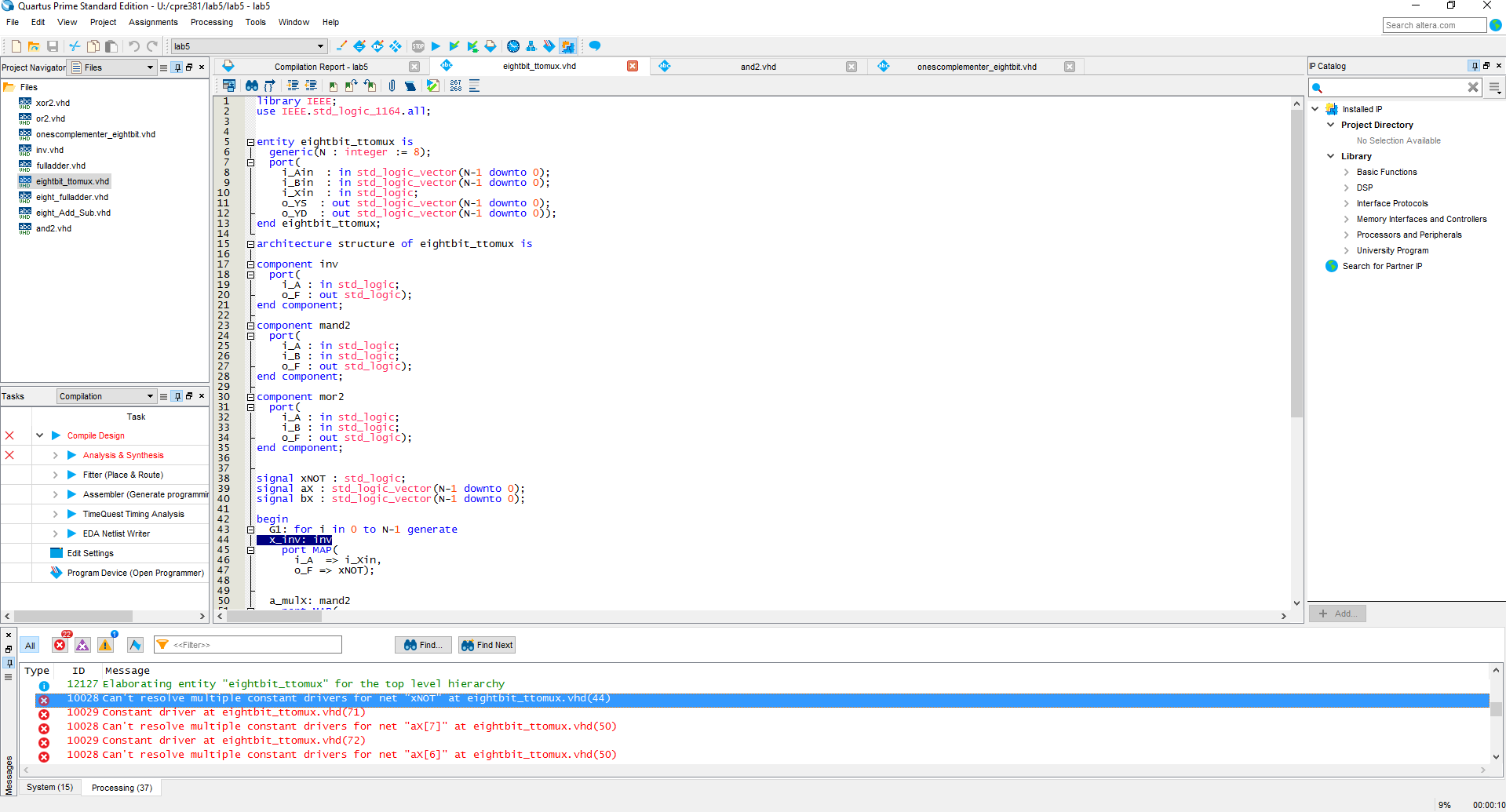
due to the problem happened in last part, I decided to write the vhdl instead of draw blocks. but I do have the block diagram drawn by hand:

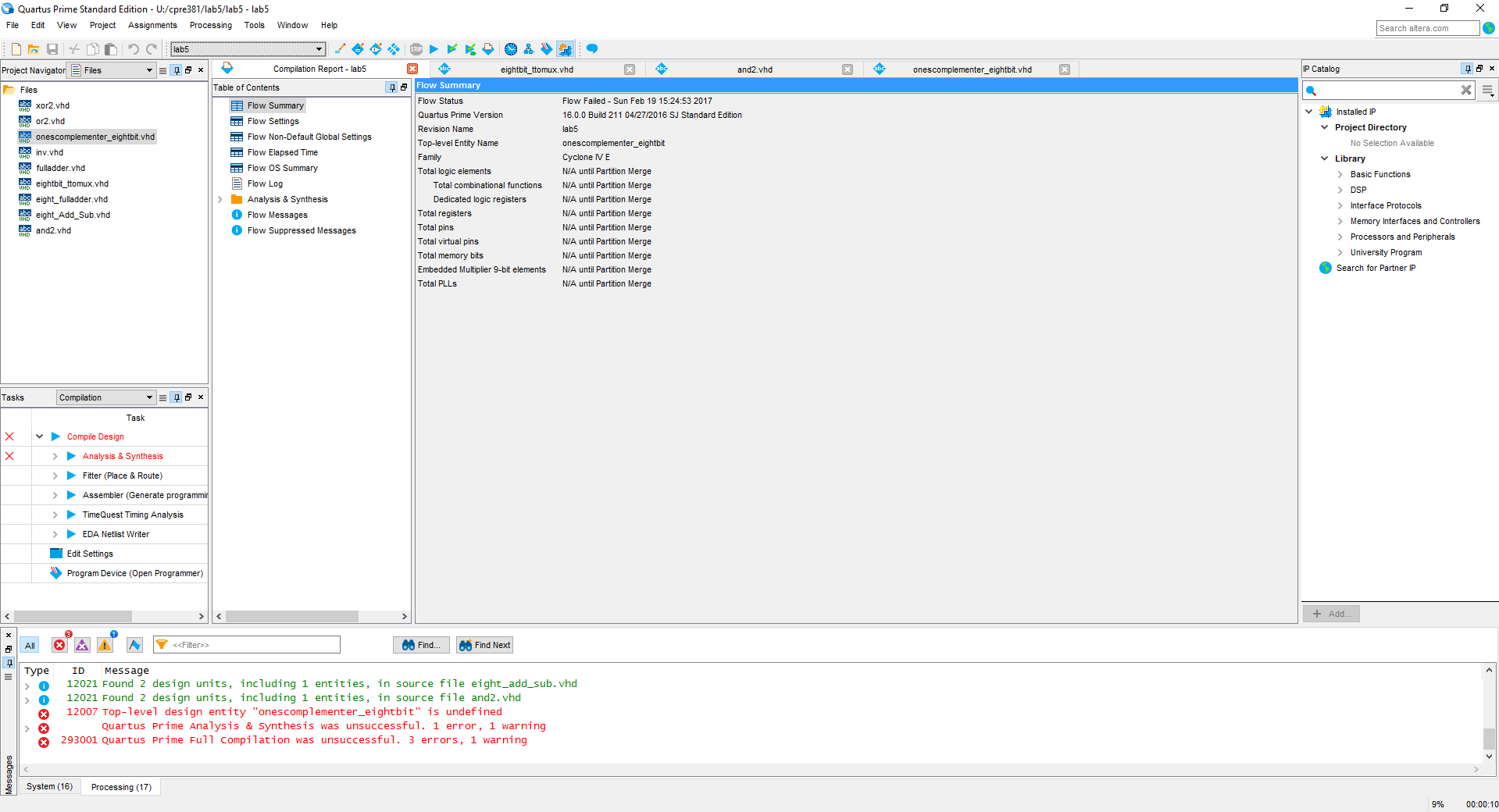


where n = 7, switch is the control signal and when it is 1, it will perform sub, 0 it will perform add. because I am using loops in vhdl, so if we want to enhance a n bit version, we only need to simply change the number of loops.

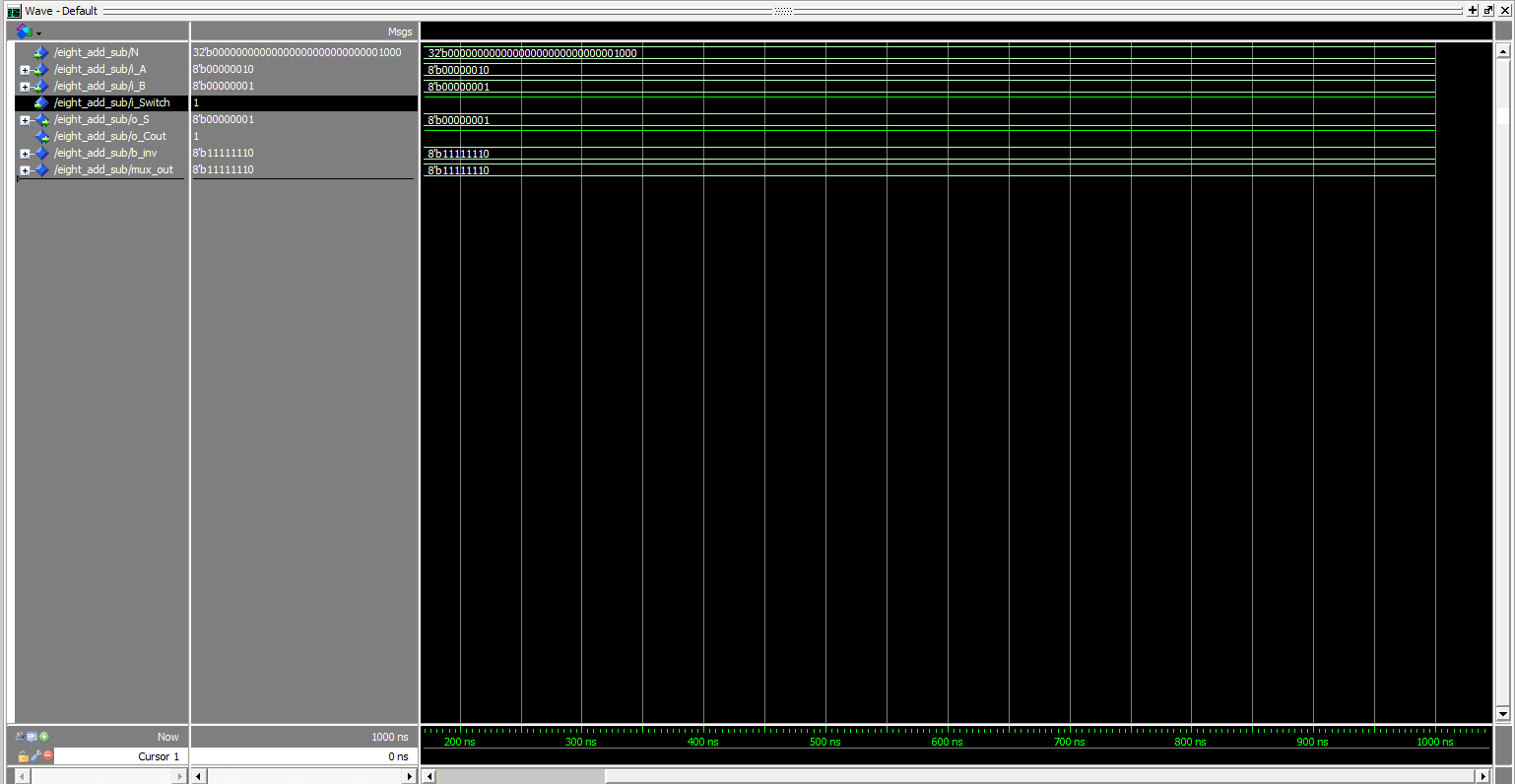
the vhdl file was named eight\_Add\_Sub.vhd.

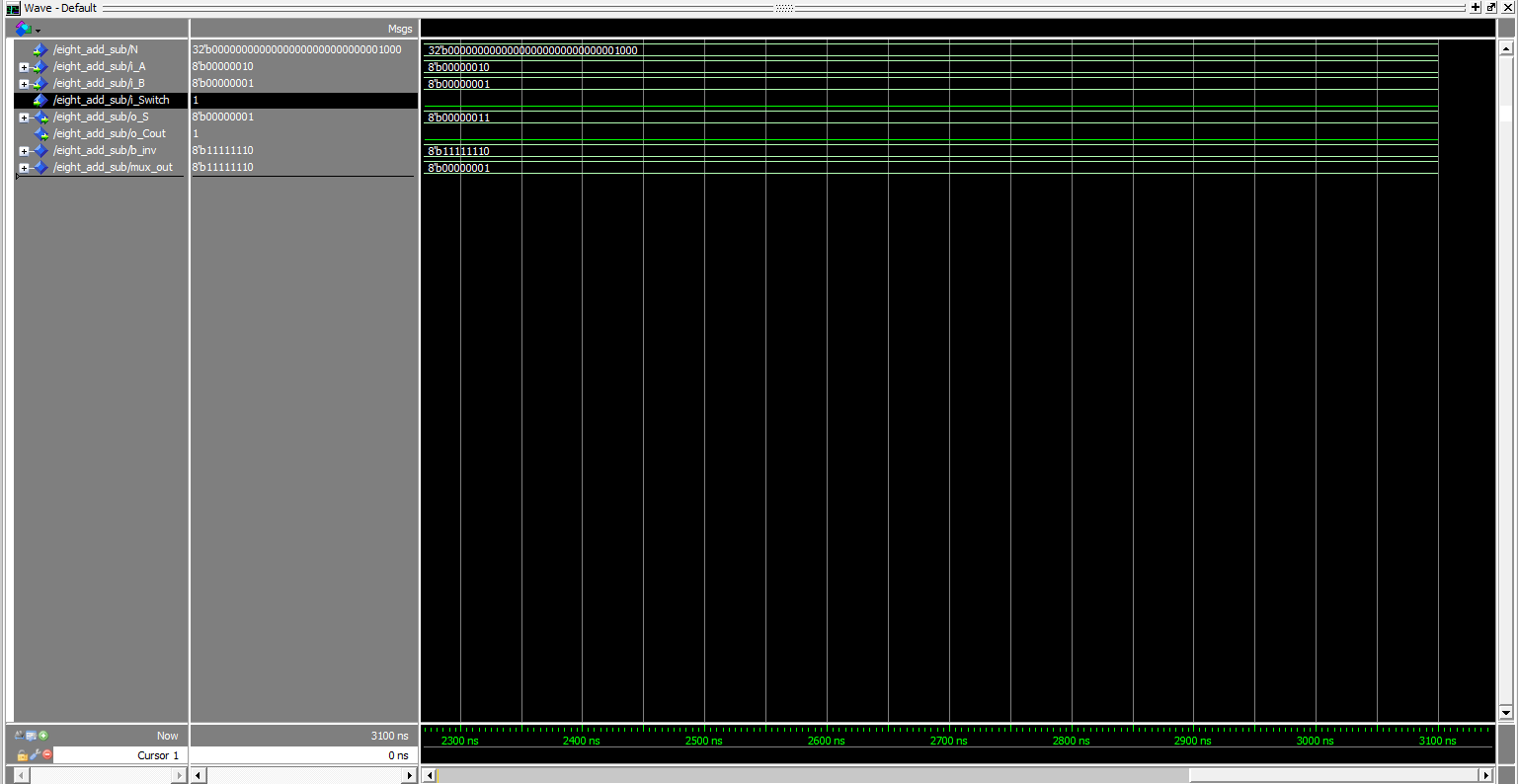
I did tried to generate a block of this program, but got errors:

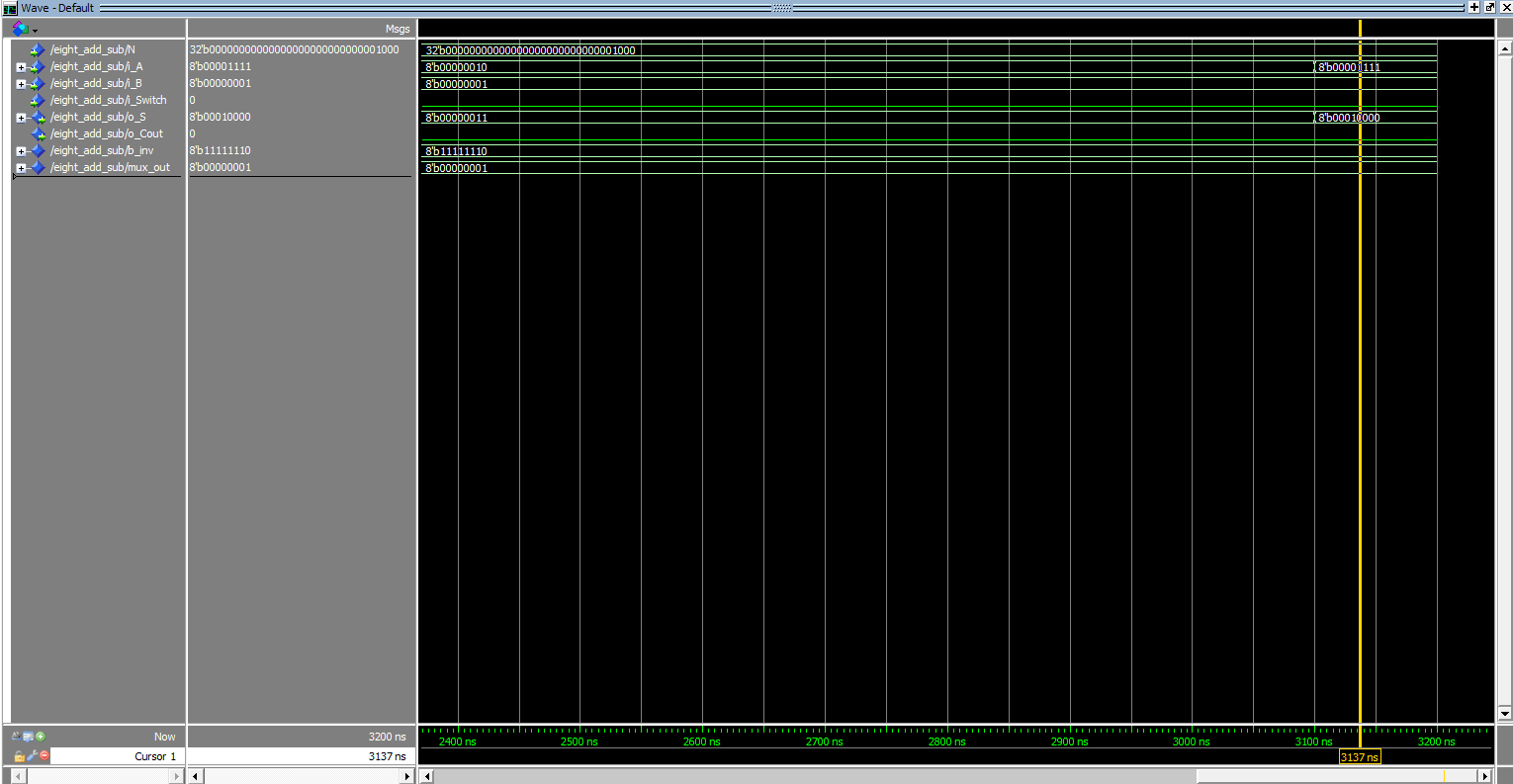


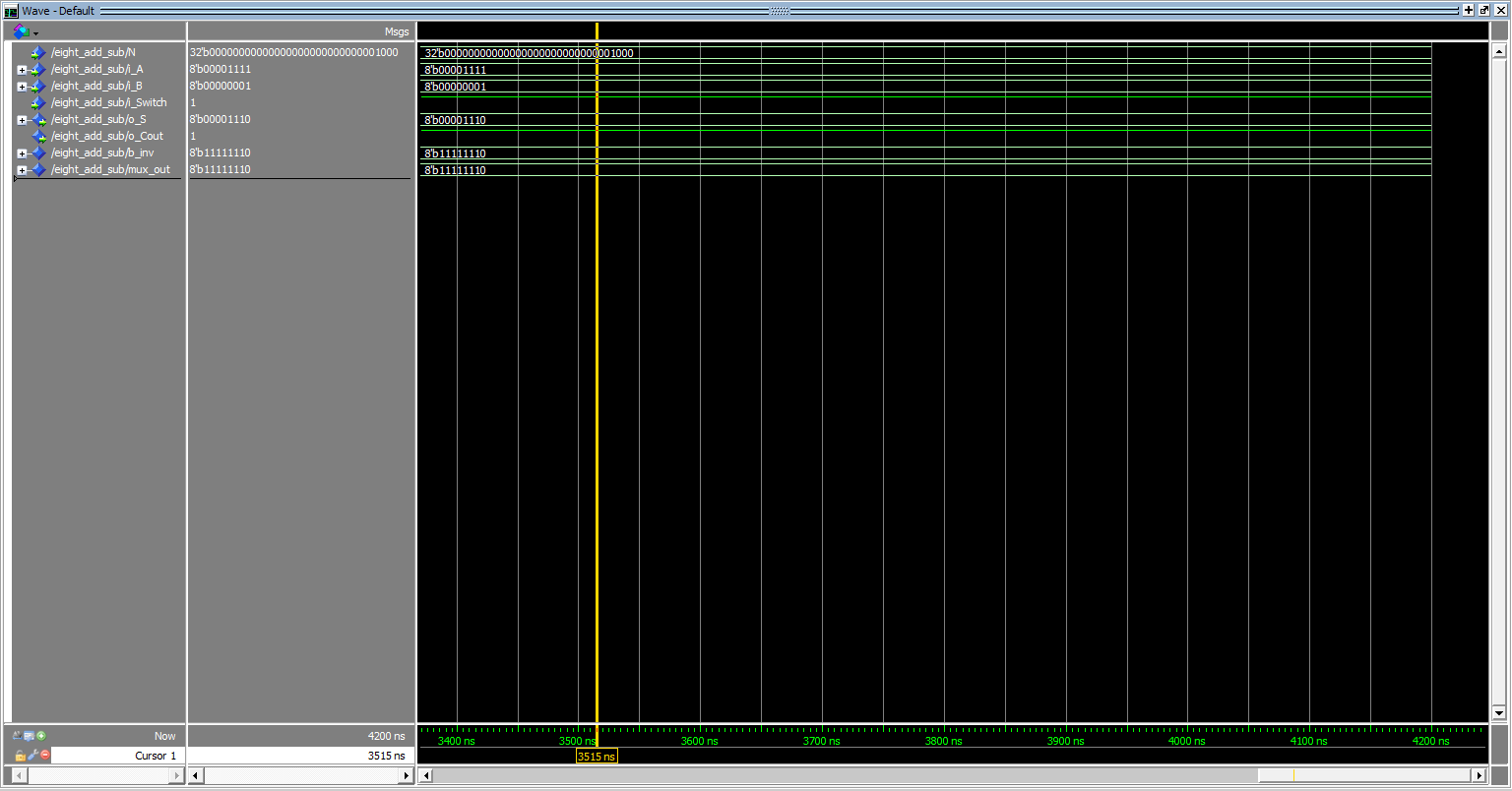


and the multi tests of waveforms:









I chose these tests because it includes all situations include add, sub, with carry and without carry.